



GR 00 P 4121

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By: [Signature]

Date: June 19, 2003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Albert Birner et al.

Applic. No. : 09/871,013

Filed : May 31, 2001

Title : Method For Making Electrical Contact With A Rear Side Of A Semiconductor Substrate During Its Processing

Examiner : William D. Coleman

Group Art Unit : 2823

11# Ext of Time 2mths &

Response

6/28/03

[Signature]

R E S P O N S E

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

Sir :

Responsive to the Office Action dated January 31, 2003, the following remarks are submitted.

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